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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,113	10/21/2003	Ehood Geva	SJO920020157US1	3731

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EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,113	GEVA ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,17-23 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,17-23, 27-28, and 30* is/are rejected.

7)☒ Claim(s) *29 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 2 pgs
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 4/28/06 has been entered. Applicants have amended the specification and claims 1-3 and 17-18. Claims 10-16 and 24-26 are cancelled. Claims 27-31 are newly added.

Specification

2. The amended specification is approved. The objections to the specification are withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9, 18, 23 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Gamand et al. (US 20020074605).

Regarding claim 1, as shown in figures 6-11, Gamand discloses a trace cover (no number) suitable for shielding a conductive trace 114 (figure 11, paragraph 85) on a circuit board (considering contained layers 12, 14, 110, 112), the circuit board inherently includes at least one circuit ground 110 (see paragraph 8), the trace cover comprising:

(a) A body 116 composed of a dielectric substrate (figure 11, paragraph 86), the body having a top surface, a bottom surface and side surfaces, the bottom surface of the body configured to be disposed substantially over the conductive trace 114 (paragraph 85); and

(b) top shielding 118 (paragraph 86) disposed on the top surface of the body, the top shielding configured to be electrically coupled with the at least one circuit ground of the circuit board (considering layer 110 as a ground layer, see paragraph 8); and

(c) wherein the trace cover is configured to be fixed to an at least partially exposed circuit board surface (surface of layer 112).

Regarding claim 2, as shown in figure 11, Gamand further discloses that side shielding 120/122 (paragraph 87) perpendiculars to the direction of the conductive trace and substantially parallel to the length of the conductive trace, the side shielding configured to be electrically coupled with the at least one circuit ground of the circuit board.

Regarding claim 3, as shown in figure 6, Gamand further discloses that at least one connecting pad (a long pad extending along the trace) such as 60/62/64/66/68/70 (paragraph 66) can be disposed on the bottom surface of the body, the connecting pad inherently configured to be soldered to a top surface of the circuit board and to electrically couple the side shielding with the at least one circuit ground. It is noted that soldering conductive elements (vias/pads for example) is old and known in the art.

Regarding claim 4, as shown in figure 8, Gamand further discloses that the side shielding can include a plurality of conductive vias 74a/78a (paragraph 71) disposed between the top surface and bottom surface of the body.

Regarding claim 5, Gamand further discloses that the plurality of conductive vias are spaced depending upon the frequency of the electric signal to be isolated (paragraph 72), thus inherently included the approximately one-quarter inch apart.

Regarding claim 6, Gamand further discloses that the side shielding includes a conductive plating (a continuous via, see paragraph 68) which disposed along the side surfaces of the body.

Regarding claim 7, Gamand discloses the top shielding 118 (conducting layer, paragraph 86), which is inherently conductive plating.

Regarding claim 8, as shown in figure 11, Gamand discloses the top shielding 118 electrically coupled to the circuit ground through the side shielding 120/122.

Regarding claim 9, as shown in paragraphs 61 and 86 and figure 11, Gamand discloses the dielectric substrate 116 (silicon dioxide) of the body is different than a dielectric substrate 112 (isolating layer) of the circuit board.

Regarding claim 18, as shown in figures 6-11, Gamand discloses every limitation as shown in claims 1 and 2 above including a trace cover suitable for suppressing electromagnetic emissions (see paragraph 1) from a conductive bus on a circuit board, the conductive bus including at least two substantially parallel bus traces 16 and 58 (see paragraph 65, noted that conductor line 114 in figure 11 can be optionally replaced by a pair of trace lines such as 16 and 58, both figures 6 and 11 are known for illustration purpose only), the circuit board including a partially exposed circuit board surface (all circuit board has exposed circuit surface) and inherently including at least one circuit ground (such as layer 110), the trace cover comprising:

(a) a body composed of a dielectric substrate 116, the body having a top surface, a bottom surface and side surfaces, the bottom surface of the body configured to be

disposed substantially over the conductive bus 114 and on the partially exposed circuit board surface (surface of 112);

(b) side shielding 120/122 perpendicular to the direction of the conductive bus and substantially parallel to the length of the conductive bus, the side shielding being electrically coupled with the at least one circuit ground of the circuit board; and

(c) top shielding 118 disposed on the top surface of the body, the top shielding being electrically coupled with the at least one circuit ground 110 of the circuit board.

Regarding claim 23, Gamand discloses every limitation as shown in claim 6 above including the side shielding which includes a conductive plating (continuous vias) disposed along side surfaces of the body.

Regarding claim 27, as shown in figures 6 and 11, Gamand discloses the trace cover inherently mechanically attached (soldering vias and conductive plate 118, for example) to a top surface of the circuit board after manufacture of the circuit board, because the conductive trace 114/16/58 must be formed first before shielding.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 17, 28 and 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gamand et al. in view of common knowledge.

Regarding claims 17, 28 and 30, Gamand discloses every limitation as shown in claims 1 and 18 above including a conductive trace 114 disposed on a circuit board (12, 14, 110, 112), means for shielding the conductive trace, and the means for shielding disposed on the outer surface of the circuit board.

But, Gamand does not disclose a plurality of circuit components disposed on the outer surface of the circuit board.

It is old and well known in the art that circuit board contains circuit components formed on or buried within the board for a complete operation of circuit board. It is noted that Gamand does not have to show other components, since the invention is centering about the shielding of a circuit trace.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have circuit components disposed on the outer surface of the circuit board (and/or buried within the board) for the complete operation of circuit board.

7. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gamand et al. in view of Jones (US 4816616).

Regarding claim 19, Gamand discloses every limitation as shown in claim 18 above, but failed to disclose bus shielding disposed within the body and between the bus traces, the bus shielding being electrically coupled with the at least one circuit ground of the circuit board.

Johns, as shown in figures 1F and 2, discloses a trace cover suitable for suppressing electromagnetic emissions from a conductive bus on a circuit board (see

column 1, lines 20-23), the conductive bus including at least two substantially parallel bus traces 30, the circuit board including at least one circuit ground G (see column 2, lines 7-10), the trace cover comprising:

(a) A body 40 (second dielectric layer) composed of a dielectric substrate.

(b) The body having a top surface (facing conductive layer 50), a bottom surface (facing the conductor traces 30 and layer 20) and side surfaces (facing conductive layer 50),

(c) The bottom surface of the body configured to be disposed substantially over the conductive bus 30, as shown in the figure 1F.

(d) As shown in figure 1F, side shielding (the section of conductive layer 50 formed along the side surfaces of the body) perpendicular to the direction of the conductive bus and substantially parallel to the length of the conductive bus (the layer 50 formed along the conductor traces 30).

(e) The side shielding being electrically coupled with the at least one circuit ground of the circuit board, see figure 2 and column 2, lines 7-10.

(f) Top shielding (the section of upper conductive reference layer 50 formed on top of layer 40) disposed on the top surface of the body, see column 3, lines 38-40.

(g) The top shielding being electrically coupled with the at least one circuit ground of the circuit board, as shown in figure 2.

(h) A bus shielding (the section of conductive layer 50 in between the conductor 30) disposed within the body and between the bus traces 30 (the conductors), and as

shown in figure 2, the bus shielding being electrically coupled with the at least one circuit ground G of the circuit board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from Jones on the circuit board of Gamand to include bus shielding disposed within the body and between the bus traces and the bus shielding being electrically coupled with the at least one circuit ground of the circuit board in order to surely protect each bus line from EMI.

Regarding claim 20, Gamand in view of Jones discloses every limitation as shown in claim 3 above including at least one connecting pad such as pads 60/62/64/66/68/70 disposed on the bottom surface of the body, the connecting pad configured to coupled the bus shielding with the at least one circuit ground.

Regarding claim 21, Gamand in view of Jones discloses every limitation as shown in claim 4 above including the bus shielding includes a plurality of conductive vias such as 74a/78a disposed between the top surface and bottom surface of the body.

Regarding claim 22, Gamand in view of Jones discloses the bus shielding is coupled to the circuit ground through the side shielding (see Jones, figures 1F).

Allowable Subject Matter

8. Claims 29 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

9. The following is a statement of reasons for the indication of allowable subject matter: The prior arts fail to teach, disclose, suggest, either alone or in combination, at least on claim 29 and 31, a trace cover which is separated and configured to be attachable to a circuit board.

Response to Arguments

10. Applicant's arguments with respect to claims 1-9, 17-23 and 27-31 have been considered but are moot in view of the new ground(s) of rejection.

Citation of Relevant Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Houghton et al. (US 6075700) disclose a method and system for controlling radio frequency radiation in microelectronic packages using heat dissipation structures.

Inoue (US 5151770) discloses a shielded semiconductor device.

Huang et al. (US 6157065) disclose an electrostatic discharge protective circuit under conductive pad.

Kumamoto et al. (US 5196920) disclose a semiconductor integrated circuit device for limiting capacitive coupling between adjacent circuit blocks.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Hoa C. Nguyen
6/29/06